IN THE CLAIMS:

Claim 1. (Previously Amended) A MOSFET logic circuit for performing a logic OR operation comprising:

~~three~~ a first and second transistors~~, first and second transistor of the three transistors~~ forming a transmission gate for outputting ~~one~~ an intermediate signal, ~~and~~ wherein at least ~~two~~ a first and second input signals are provided to the first and second transistors~~,~~; and

a third transistor for providing an output to be combined with said intermediate signal to create an output signal indicative of an OR operation performed on ~~a~~ said first and second ~~input signal of the at least two~~ input signals ~~is~~, said output signal is output from the MOSFET logic circuit to any static CMOS logic gate.

Claim 2. (Currently Amended) The MOSFET logic circuit as in claim 1, wherein the ~~three~~ said first and third transistors are ~~include first and second~~ PMOS transistors and ~~one~~ said second transistor is a NMOS transistor.

Claim 4. (Currently Amended) The MOSFET logic circuit as in claim 1, wherein the first input signal is provided to a source of first and second transistors ~~of the three transistors~~, the second input signal is provided to a gate of the second transistor, and a complement of the second input signal is provided to a gate of the first transistor.

Claim 5. (Currently Amended) The MOSFET logic circuit as in claim 1, wherein a complement of the second input is provided to a gate of a third transistor ~~of the three transistors~~.

Claim 6. (Currently Amended) The MOSFET logic circuit as in claim 1, ~~wherein the at least two input signals to the first and second transistors~~ further providing a third input signal to said third transistor, said third input signal being ~~comprise~~ a complement of the second input signal.

Claim 7. (Previously Amended) The MOSFET logic circuit as in claim 1, wherein when the second input signal has a logic LOW level the output of the MOSFET logic circuit is an output signal of the transmission gate.

Claim 8. (Currently Amended) The MOSFET logic circuit as in claim 1, wherein ~~a~~ the third transistor of the three transistors is a pull-up transistor, and when the second input signal has a logic HIGH level the output of the MOSFET logic circuit has a voltage level approximately equal to a drain of the third transistor, which pulls up the output signal from the transmission gate to a logic HIGH level.

Claim 9. (Currently Amended) The MOSFET logic circuit as in claim 1, wherein a delay of the MOSFET logic circuit is one of a delay of ~~a~~ the transmission gate formed by first and second transistors of the three transistors, and a delay of a third transistor ~~of the three transistors~~.

Claim 10. (New) A logic OR circuit comprising:

a transmission gate for outputting a first intermediate output signal, said transmission gate being formed by a pMOS transistor receiving a first input signal and a nMOS transistor receiving a first input signal, wherein a gate of said pMOS transistor receives a second input signal; and

a pull-up pMOS transistor receiving a complement of said second input signal, said pull-up pMOS transistor providing a second intermediate output signal for combining with said first intermediate output signal to create an OR output signal,

wherein said OR output signal is indicative of an OR operation performed on said first and second input signals, said OR output signal is output from the OR logic circuit to any static CMOS logic gate.